AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(currently amended)** A chip scale package, comprising:

~~a plurality of terminals for making external electrical connections;~~

a chip having a plurality of bonding pads on an active surface thereof, ~~the bonding pads electrically connected to the terminals,~~ wherein a backside surface of the chip is exposed from a surface of the chip scale package; ~~and~~

a redistribution layer disposed on the active surface of the chip;

a plurality of terminals for making external electrical connections, the terminals disposed on the redistribution layer and electrically connected to the bonding pads; and

an ink mark formed on the backside surface of the chip.

2. **(currently amended)** A method [[for]] of marking wafer-level chip scale packages, the method comprising the ~~following~~ steps of:

providing a wafer having a plurality of dice formed thereon, wherein the dice have been packaged into a plurality of semi-finished chip scale packages, wherein each of the semi-finished chip scale packages comprises a plurality of terminals for making external electrical connections, each die has a plurality of bonding pads on an active surface thereof, the bonding pads are electrically connected to the respective terminals, and a backside surface of each die is exposed from a surface of the respective semi-finished chip scale ~~packages~~ package;

positioning the semi-finished chip scale packages formed on the wafer;

printing ink marks by transferring ink from a printing device onto [[on]] the exposed backside ~~surface~~ surfaces of the dice;

curing the ink marks on the dice; and

dicing the wafer to obtain a plurality of separated chip scale packages ~~wherein each package is separated from other packages~~.

3. **(currently amended)** The method as claimed in claim 2, further comprising [[a]] the step of removing defective ink marks after the printing step and before the curing step.

4. **(currently amended)** The method as claimed in claim 2, wherein the positioning step is performed by a positioning device ~~and the printing step is performed by a printing device~~, the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device.

5. **(currently amended)** The method as claimed in claim 2, wherein the wafer has a plurality of dicing streets between the semi-finished chip scale packages, and the ~~position~~ positioning step is performed by finding the dicing street with a charge coupled device (CCD).

6. **(currently amended)** The method as claimed in claim 5, wherein the positioning step is performed by a positioning device ~~and the printing step is performed by a printing device~~, the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device.

7. **(currently amended)** A semiconductor wafer, comprising a plurality of dice wherein each of said dice has

a plurality of bonding pads on an active surface thereof,

a redistribution layer disposed on the active surface,

a plurality of terminals for making external electrical connections disposed on the redistribution layer and electrically connected to the bonding pads, and

an ink mark on a backside surface thereof.

8. **(currently amended)** A semiconductor die, comprising:

a plurality of bonding pads on an active surface thereof,

a redistribution layer disposed on the active surface,

a plurality of terminals for making external electrical connections disposed on the redistribution layer and electrically connected to the bonding pads, and

an ink mark on a backside surface thereof.

9. **(new)** The method as claimed in claim 2, wherein the printing step is performed by printing the backside surfaces of all of the dice in one action.

10. **(new)** The method as claimed in claim 2, wherein all of the semi-finished chip scale packages are positioned simultaneously.

11. **(new)** The method as claimed in claim 2, wherein the positioning step and the printing step are performed synchronously.

12. **(new)** The method as claimed in claim 2, wherein the printing step comprising the step of applying ink in a recognizable pattern directly on the exposed backside surface surfaces of the dice to form said ink marks.

13. **(new)** The method as claimed in claim 2, wherein the printing step comprising the

step of applying ink in a recognizable pattern indicative of an identifier of each said die directly on the exposed backside surface of the die.